Outline

- **Part I – see slides from last mtg (24 Oct 2003)**

- **Part II – Run IIb L1 CAL Upgrade**
  - Motivation for Trigger Upgrade
  - Goals for L1 CAL Upgrade
  - Interlude – Acronyms and Abbreviations
  - Run IIa Limitations
  - Run IIb Solutions
  - Run IIb L1 CAL System
  - The Players
  - Racks, Crates and Cables
  - L1 Triggering
  - SCL Interface Card
  - Action Items

Motivation for Trigger Upgrade

Trigger	Run IIa Definition	Example Channel	L1 Rate [kHz] (no upgrade)	L1 Rate [kHz] (w/ upgrade)
EM	1 EM TT > 10 GeV	W® ev WH® evjj	1.3	0.7
DiEM	1 EM TT > 7 GeV 2 EM TT > 5 GeV	Z® ee ZH® eejj	0.5	0.1
Muon	1 Mu Pt > 11 GeV CFT Track	W® mv WH® mvjj	6	1.1
Di-Mu	2 Mu Pt > 3 GeV CFT Tracks	Z/y ® mm ZH® mmjj	0.4	<0.1
e + Jets	1 EM TT > 7 GeV 2 Had TT > 5 GeV	WH® evjj tt® ev+jets	0.8	0.2
Mu + Jet	1 Mu Pt > 3 GeV 1 Had TT > 5 GeV	WH® mvjj tt® mv+jets	<0.1	<0.1
Jet+MEt	2 TT > 5 GeV MEt > 10 GeV	ZH® vvbb	2.1	0.8
Mu+EM	1 Mu Pt > 3 GeV + Trk 1 EM TT > 5 GeV	H® WW,ZZ	<0.1	<0.1
Iso Trk	1 Iso Trk Pt > 10 GeV	H® tt , W® mv	17	1.0
Di-Trk	1 Iso Trk Pt > 10 GeV 2 Trk Pt > 5 GeV 1 Trk matched w/ EM	H® tt	0.6	<0.1
Total Rate Cal Rate			~30 4.7	3.9 1.8

Luminosity
2´10^{32}

Beam Crossing (BC)
396 ns

L1 Limit
~3 kHz

Goals for L1CAL Upgrade

1. Improved capability to correctly assign the calorimeter energy to the correct bunch crossing via digital filtering
2. Significantly sharper turn-on for jet triggers
3. Improved trigger turn-on for EM objects
4. Ability to make shape and isolation cuts on EM triggers
5. Ability to match tracks to energy deposition in calorimeter trigger towers
6. Ability to include energy in the intercryostat reagion (ICR) when calculating jet energies and the missing ET
7. Ability to add topological triggers which will aid in triggerin on specific Higgs final states

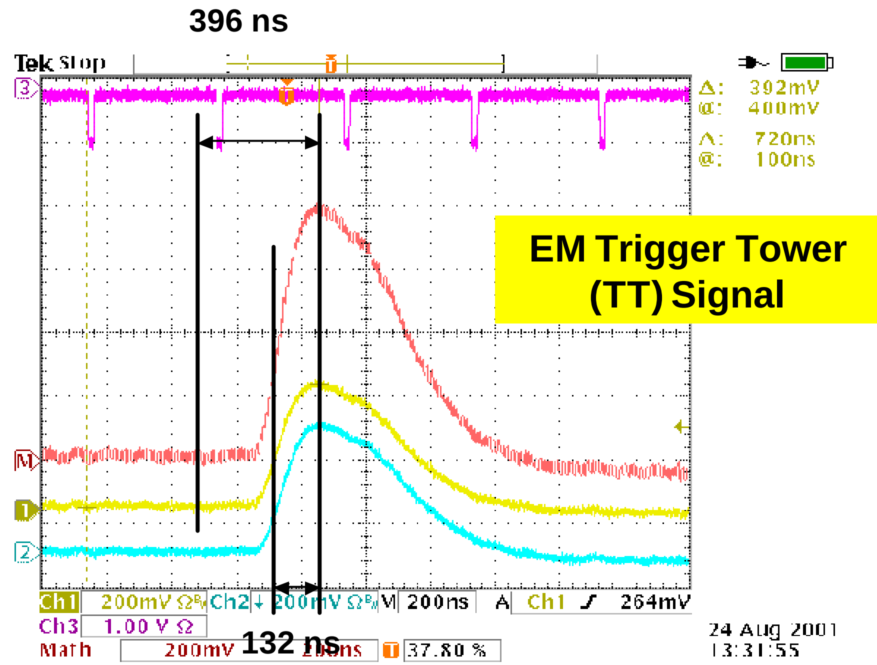
Items 2, 4 and 5 will help reduce overall rates

Copied from Technical Design Report for Run IIb Trigger Upgrade

Acronyms and Abbreviations

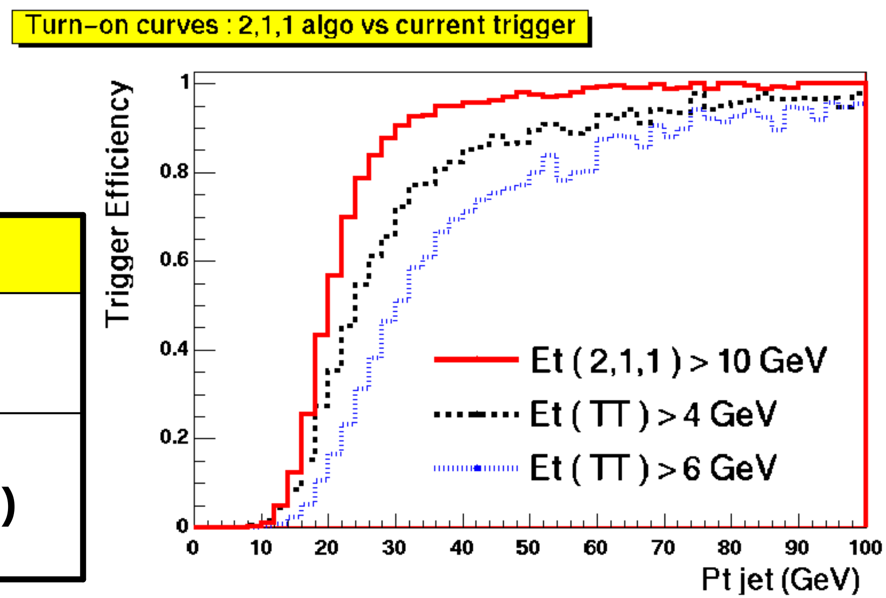
- ADF: ADC & Digital Filter Card
  - Run IIb L1Cal card that digitizes and filters analog signals from BLS
- ADF Timing (aka SCL Interface)
  - Run IIb L1Cal card that distributes SCL signals to ADFs
- BLS: BaseLine Subtractor Card
  - Run IIa/IIb card that constructs analog TT signals from calorimeter cell signals (in collision hall)
- CTFE: Calorimeter Trigger Front End Card
  - Run IIa card that digitizes BLS signals, counts TTs over threshold and does first stage of Et summing (in MCH1)
- GAB: Global Algorithm Board
  - Run IIb card that collects TAB outputs, constructs trigger terms and transmits them to the TFW
- LVDS: Low Voltage Differential Signal
  - Serial data transmission protocol used for communication between Run IIb L1Cal components
- MCH: Movable Counting House
  - MCH-1 (1^{st} floor) houses L1Cal. This is accessible during data taking.
- SCL: Serial Command Link
  - Means of communicating D0 TFW timing and control signals to all parts of D0 Trigger/DAQ
- Splitter
  - Splits analog signals from BLS (at CTFE) for Run IIb L1Cal studies
- TAB: Trigger Algorithm Board
  - Run IIb card that performs sliding windows and Et summing algorithms on ADF outputs
- TFW: Trigger Framework
  - System that collects trigger terms from all D0 trigger systems, makes final trigger decisions and distributes timing and control
- TT: Trigger Tower
  - 0.2x0.2 (hxf) region of calorimeter cells (EM or Hadronic) used as input to L1Cal
- VME/SCL Card
  - Run IIb card that interfaces TABs/GABs to VME using a custom serial protocol and distributes SLC signals to the TABs/GABs

Run IIa Limitations



- Signal rise > 132 ns
  - cross threshold before peak
    - trigger on wrong crossing
  - affects high-Et events
  - prevents 132 ns running

- Poor Et-resolution (Jet,EM,MEt)
  - slow turn-on curves
    - 5 GeV TT threshold Þ 80% efficient for 40 GeV jets
  - low thresholds
    - unacceptable rates at *L* = 2´10^{32}

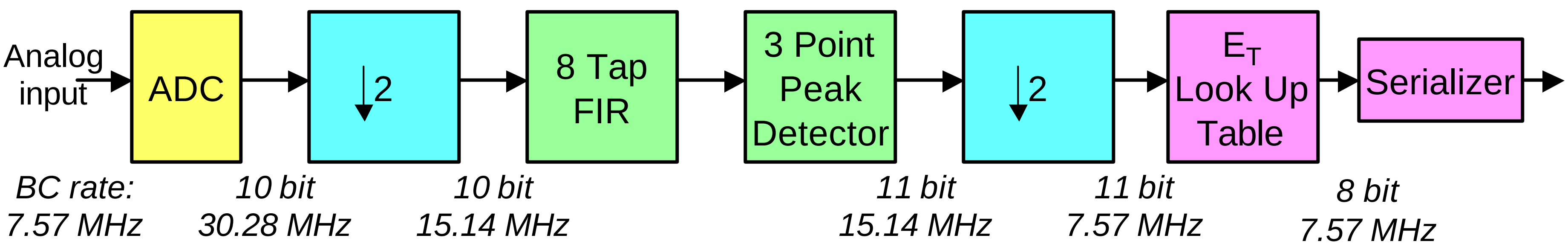


Trigger	Phys. Chan	Rate (kHz)
EM Trigger 1 TT>10 GeV	W ® ev	1.3
Jet Trigger 2 TT>5 GeV + MEt>10 GeV	ZH ® vvbb	2.1 (L = 2e32)

Solution to Signal Rise Time

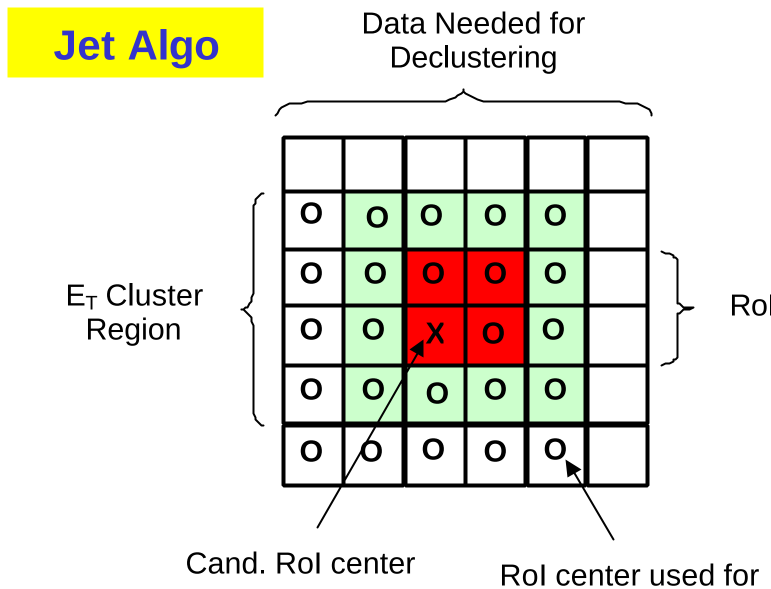
- **Solution to Signal Rise Time: <u>Digital Filtering</u>**
  - **digitize Calorimeter trigger signals**
  - **8-tap Finite Impulse Response (FIR) digital filter (6-bit coefficients) + Peak Detector run at BC´2**
  - **reformats output for transmission to physics algorithm (algo) stage**
- **Benefits**
  - **allows running at 132 ns (keeps this option open)**
  - **improvements in energy resolution (under study)**
  - **note: this stage is necessary as input to algo stage**

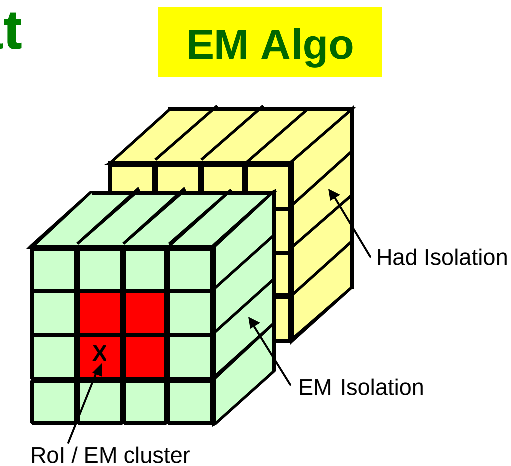
ADC & Digital Filter (ADF) Processing Chain

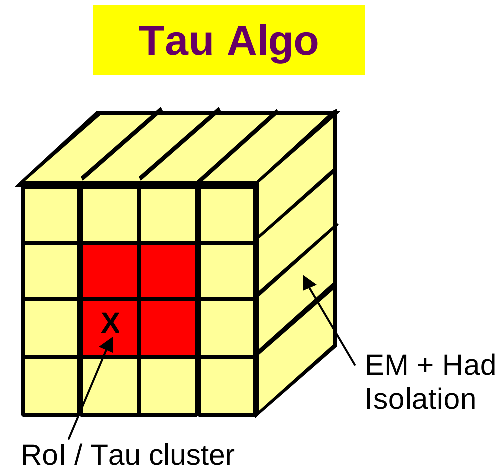


Solution to Rate Problem

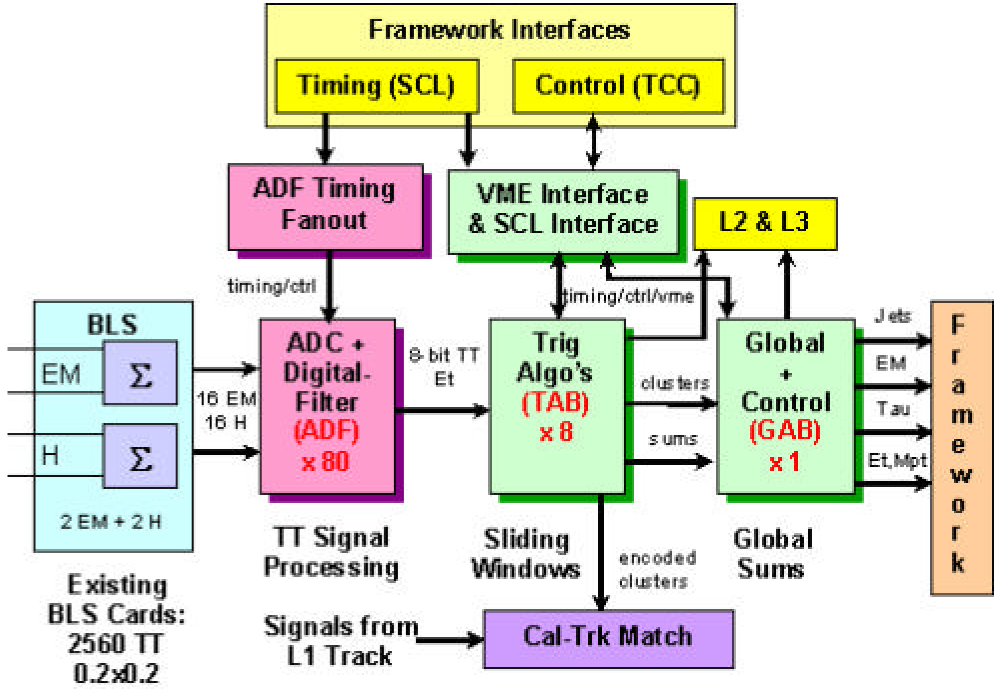
- Sliding Windows Algorithm
  - Et cluster local maximum search on 40´32 (h´f) TT grid
  - Jet, EM & Tau algo's
  - Better calculation of missing Et
  - Topological Triggers
  - Jet, EM clust output for matching with L1 Tracks
- Benefits
  - ´2.5-3 Jet Rate reduction at constant efficiency
    - ZH→*vv*bb Rate: 2.1→0.8 kHz
  - Similar gains for EM &Tau
  - MEt, Topological Triggers under study







The Run IIb L1Cal System



Custom Board	No	Purpose
ADF: ACD/Dig. Filt.	80	digitize, filter, E-to-Et
ADF Timing Fanout	4	ADF control/timing
TAB: Trig Algo Board	8	algo's, Cal-Trk out, sums
GAB: Global Algo Board	1	sums, trigs to FWK
VME/SCL Board	1	VME comm & timing fanout to TAB/GAB

The L1Cal Team

Saclay — ADFs/ADF Timing/Splitters
- Physicists: J.Bystricky, P.LeDu*, E.Perez
- Engineers: D.Calvet, Saclay Staff

Columbia/Nevis — TABs/GABs/VME-SCL
- Physicists: H.Evans*, C.Johnson, J.Parsons, J.Mitrevski
- Engineers: J.Ban, B.Sippach, Nevis Staff

Michigan State — Framework/Online Software
- Physicists: M.Abolins*, C.Brock, H.Weerts
- Engineers: D.Edmunds, P.Laurens

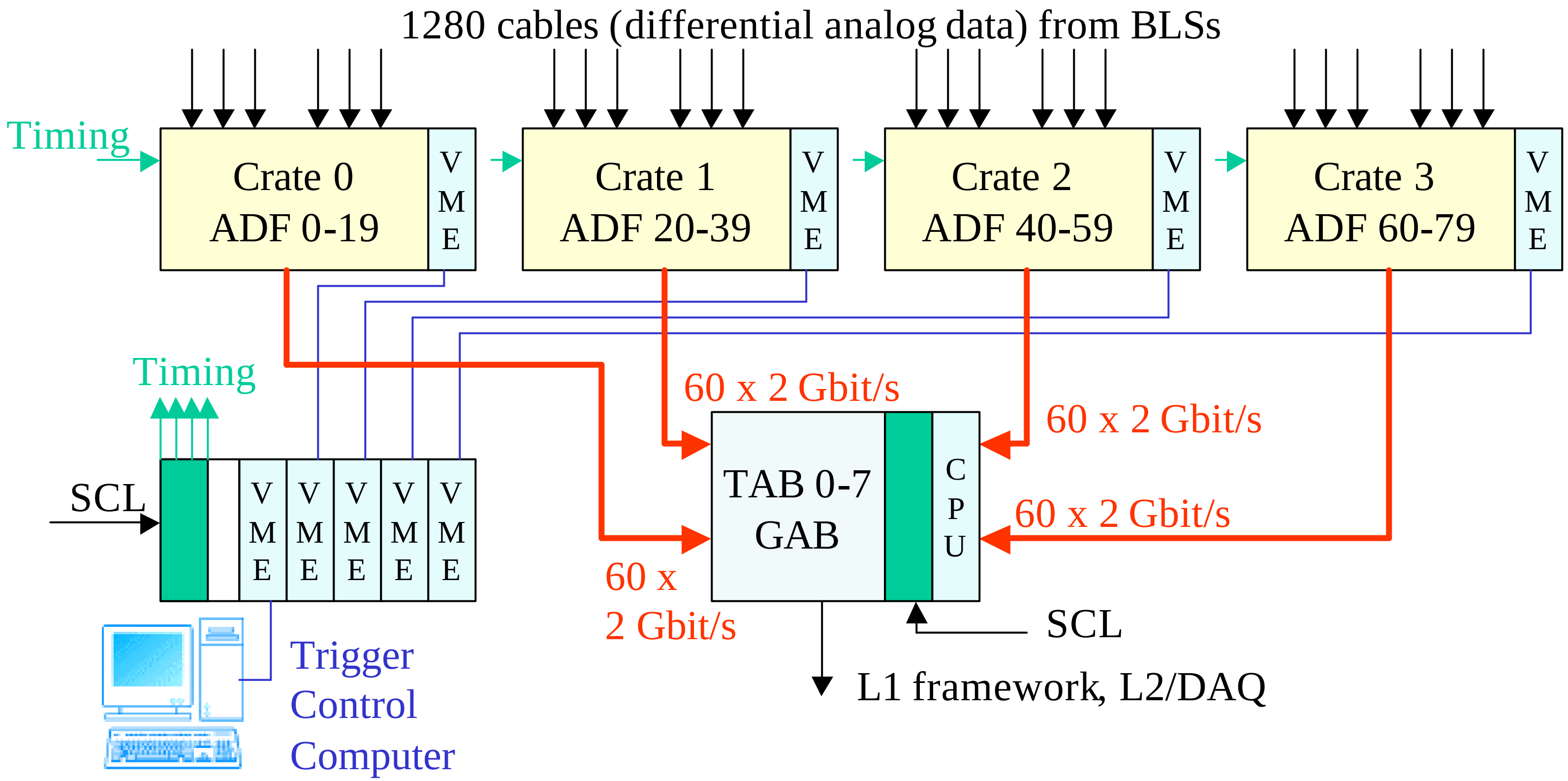
Northeastern — Online Software
- Physicists: D.Wood

Fermilab — Test Waveform Generator
- Engineers: G.Cancelo, V.Pavlicek, S.Rapisarda

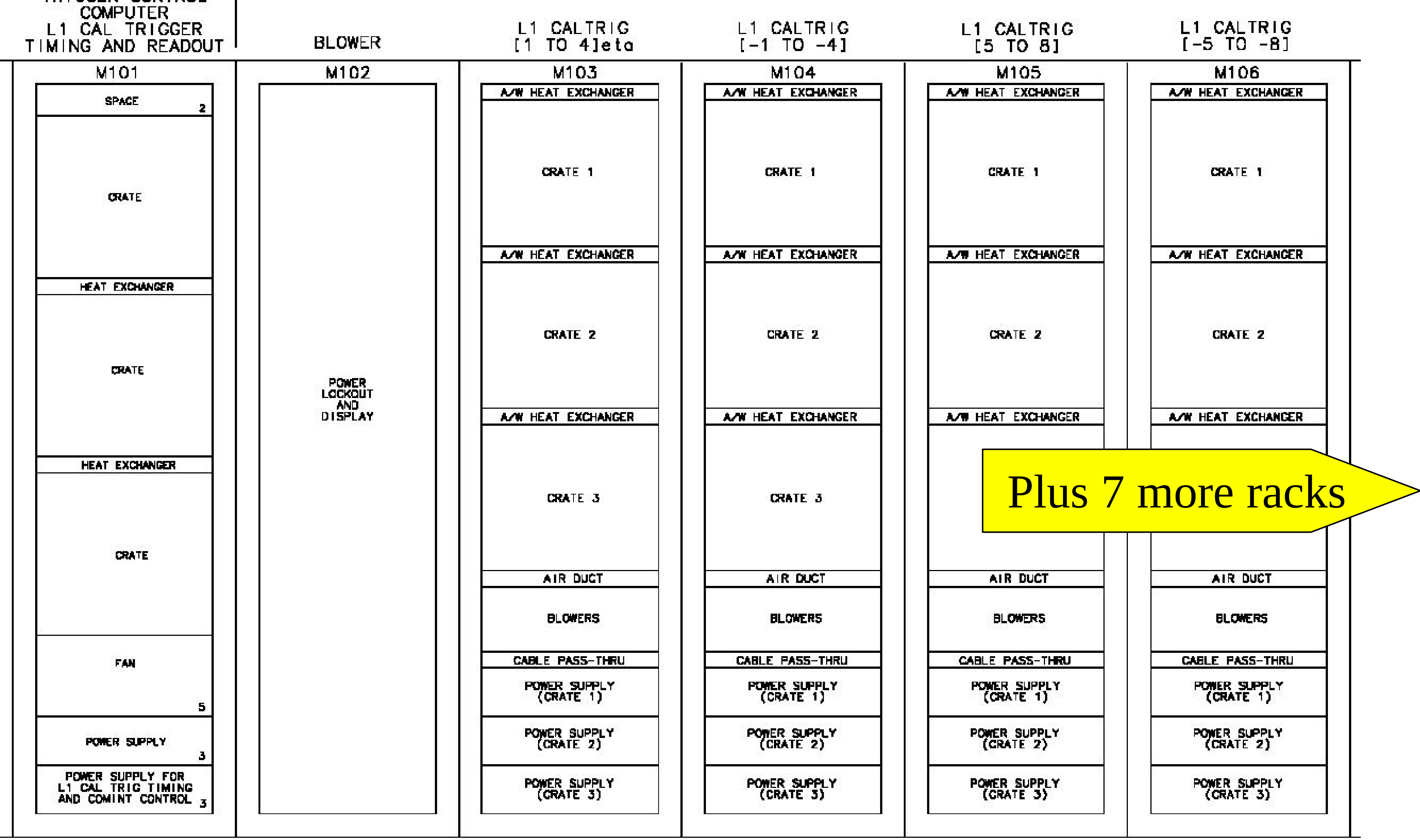
UIC — SCLIF/Cabling/Commissioning
- Physicists: N.Varelas, M.Adams, A.Stone, M.Camuyrano
- Engineers: C.Pellegrini

* L1Cal Project Leaders

ADF System



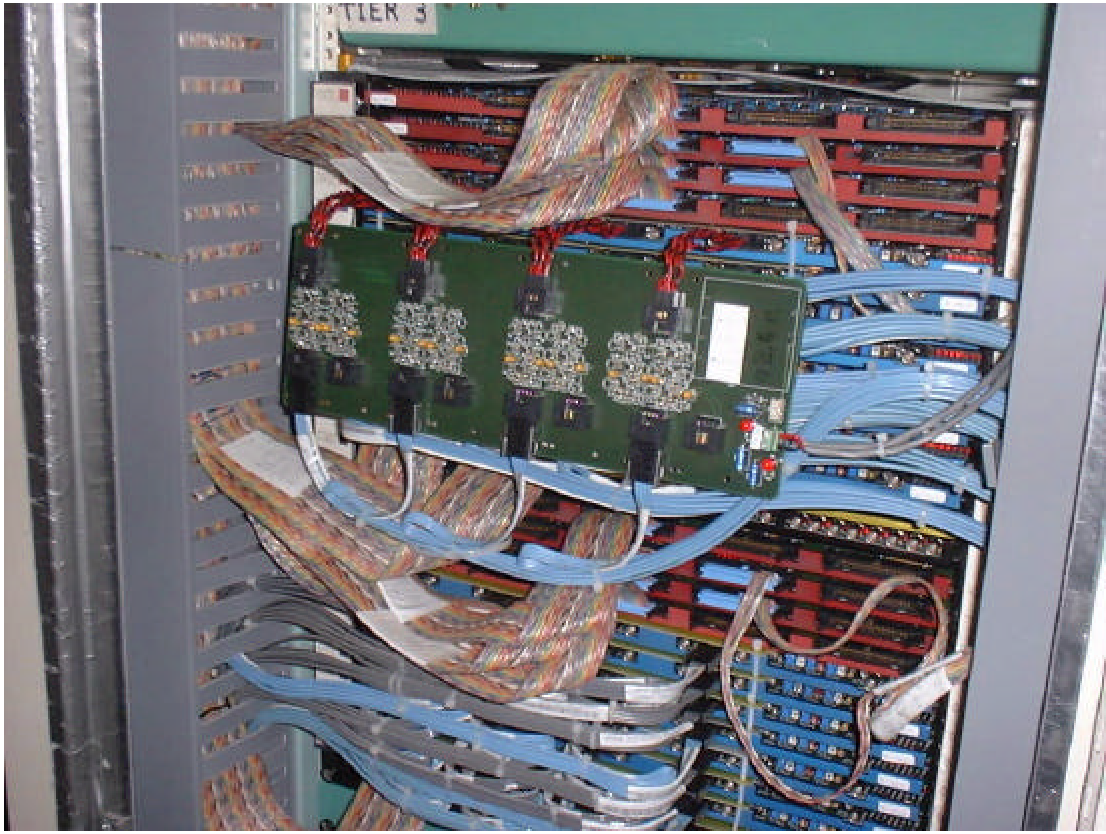
- **32 analog channels + 3 output 2 Gbit/s per ADF board**
- **20 ADF boards+ 1 interface per crate (« VME Interconnect »)**
- **80 ADF boards in 4 VME crates in total**
- **1 board for timing distribution**



Disconnect all cables, protect & preserve for upgrade. The Run I L1 CAL rack layout did not change for Run IIa. For Run IIb, there are only four crates of electronics, not 13 racks! The cabling for the upgrade will likely require patch panel (input old cables, ouput new cables). UIC can contribute the manpower to the mapping, cabling and commissioning.

Run IIa Rack & Cables w/Splitter

- **Access to Real TT Data using "Splitter" Boards**
  - **designed/built by Saclay**
  - **active split of analog signals at CTFE input**
  - **4 TTs per board**
  - **installed: Jan. 2003**



- **Splitter Data**
  - **no perturbation of Run IIa L1Cal signals**
  - **allows tests of digital filter algorithm with real data**

Types of L1 Trigger for ADF System

- **D0 Framework L1 Accept**
  - *Generated by D0 framework; sent to all Geographic Sections via SCL*
  - *Fanout to ADF system by SCL Interface Fanout card (SCLIF)*
  - *Indicates that current BC is a L1 accepted event*

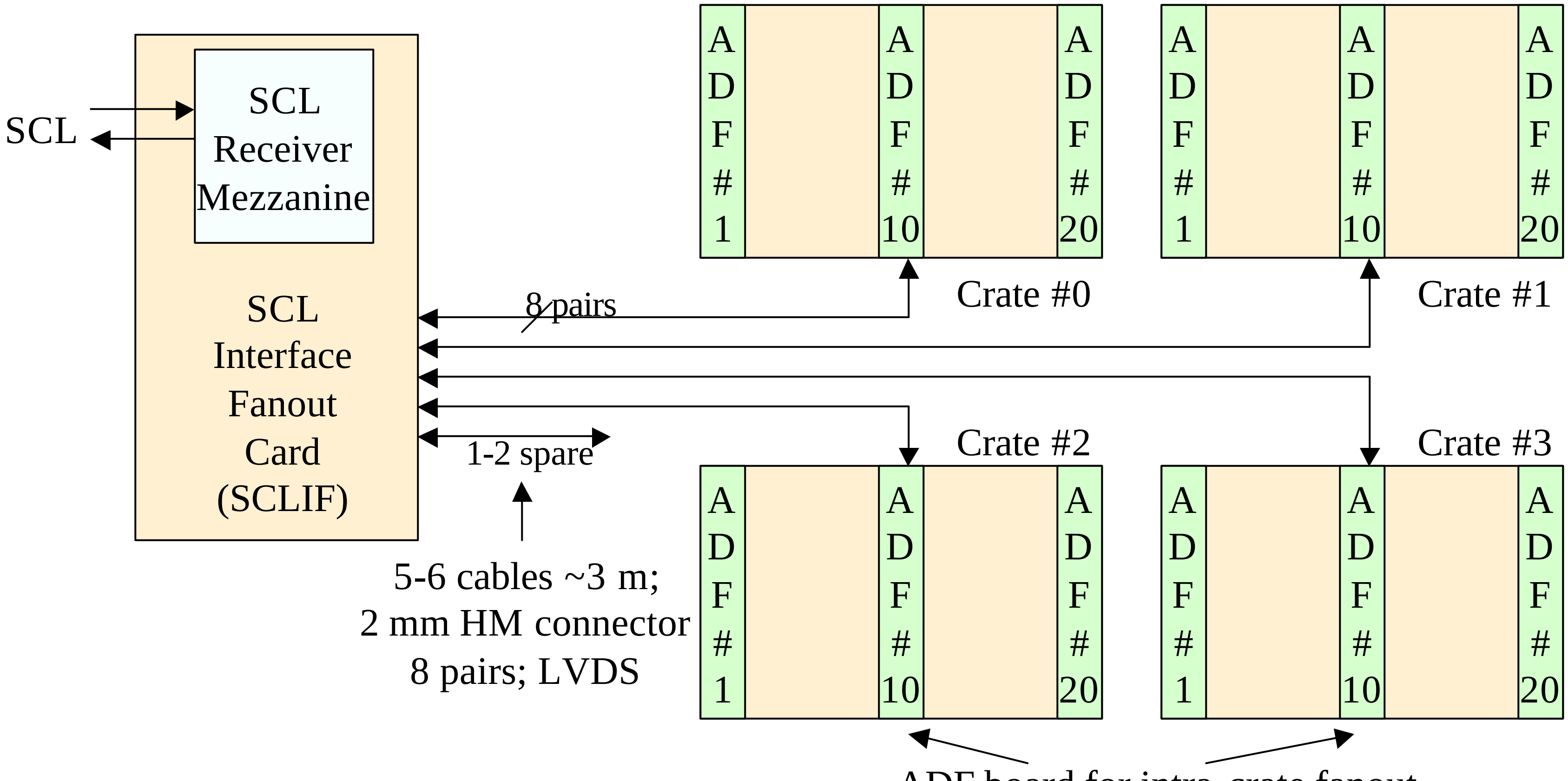
- **L1 Accept with Monitoring**
  - *Generated asynchronously by TCC to indicate that monitoring data of Geo section should be kept for one of next D0 framework L1 Accept*
  - *Sent synchronously by D0 L1 framework to Geo section by L1 Qualifier*
  - *If L1 Framework accept and L1 Qualifier for Monitoring asserted: the current L1 is to be monitored; all history data kept for TCC readout*
  - *L1 accept with monitoring flags are fanout to ADF system by SCL Interface Fanout Card*

Types of L1 Trigger for ADF System

- **L1 Software Accept**
  - *Generated asynchronously by TCC to indicate that one of the next L1 crossing should be treated as D0 Framework L1 Accept by ADF system*
  - *Issued by one ADF card upon asynchronous write by TCC,*
  - *bounced-back synchronously to ADF system by SCLIF card*

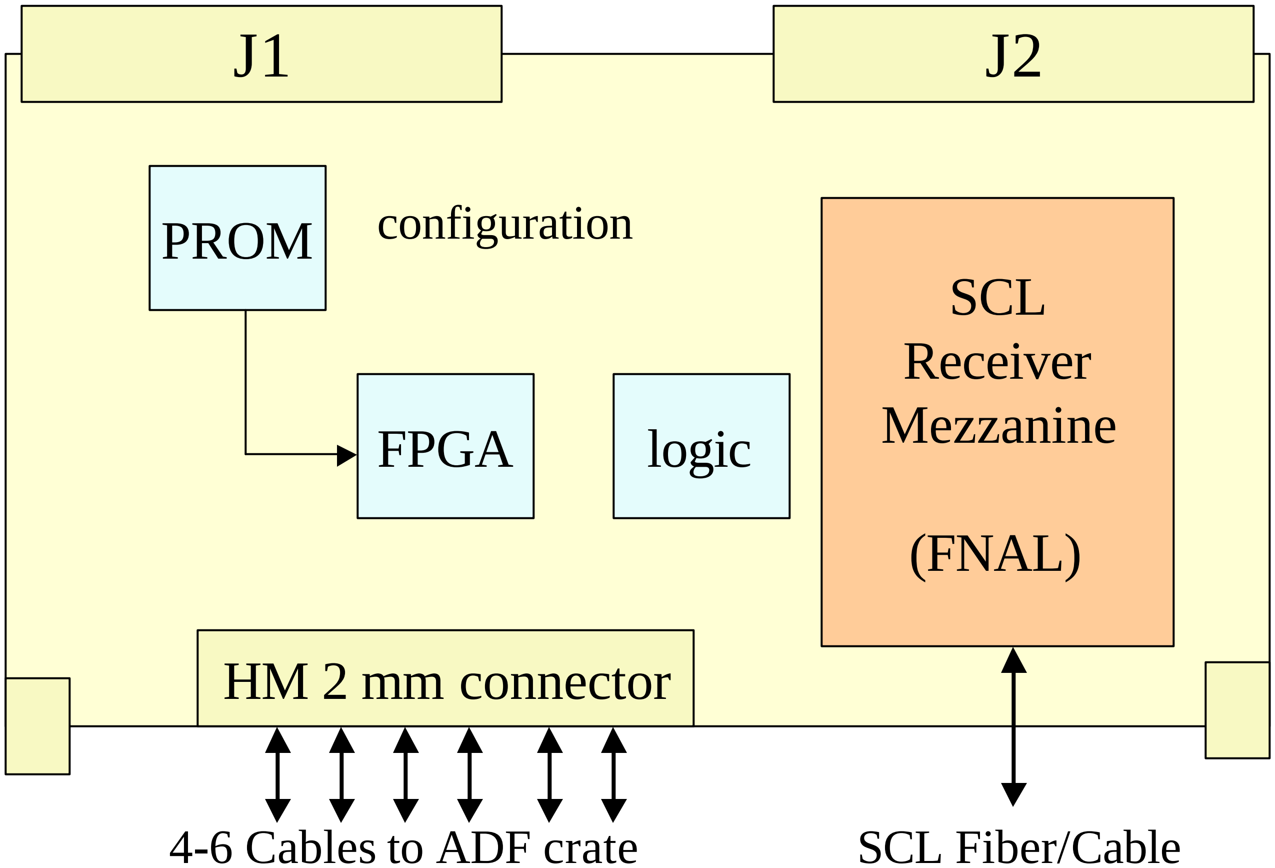
- **L1 Self trigger Accept**
  - *Generated by each ADF channel when ADC input greater than programmable threshold*
  - *Wired-Ored for all channels on an ADF card*
  - *Wired-Ored for all ADF cards within each ADF crate and sent to SCLIF*
  - *OR-ed by SCLIF and sent back to all ADF cards synchronously*

SCL signals fanout



- **1 cable to one ADF board in each ADF crate**
- **ADF board where cable is plugged in charge of fanout within crate**

SCL Interface and Fanout card



- VHDL design in progress
- 3U or 6U mechanics; No slow control
- No slot available in ADF crate -> back of slot 0 if enough space

Selected Schedule Milestones

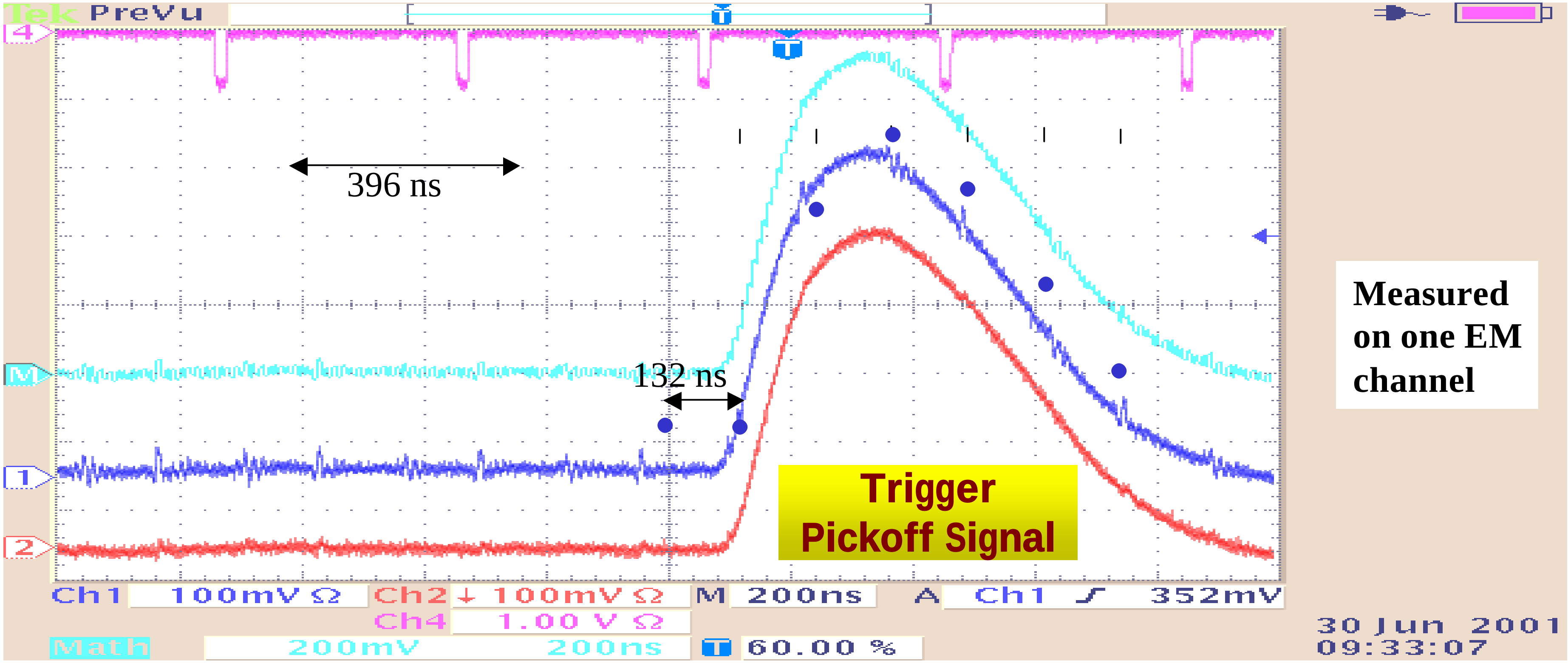
Milestone	Curr. Sched End	Lehman End
TAB Prototype (bench tested)	8/29/03	5/16/03
ADF Prototype (bench tested)	10/7/03	5/2/03
VME/SCL (bench tested)	6/17/04	¾
GAB Prototype (bench tested)	1/30/04	7/16/03
Prototype Integration Tests	1/26/04	10/9/03
Pre-Production Integration	10/1/04	5/5/04
Production Readiness Review	10/8/04	5/12/04
TAB Production (bench tested)	3/25/05	10/18/04
ADF Production (bench tested)	5/13/05	12/8/04
GAB Production (bench tested)	7/5/05	2/7/05
L1Cal Production Complete	7/5/05	2/7/05

- Main Cause of Delays   Complicated Design & Layout of ADF & TAB
- Integration Success   More time at Prototype Stage Worth the Effort

Next Time

- SCL Interface Card
  - When is a prototype needed?
  - Is this something that Craig can do?
  - Where can I, Mario et al. assist in the test stand?
  - More details/documentation from Denis Calvet…
- Cabling
  - Will speak to Dan and work out a plan of action
    - This week was not good – Trigger Framework issues
  - The design and mapping – this is something we can work on
    - Touching the cables will not happen for two years

Run IIa Limitation



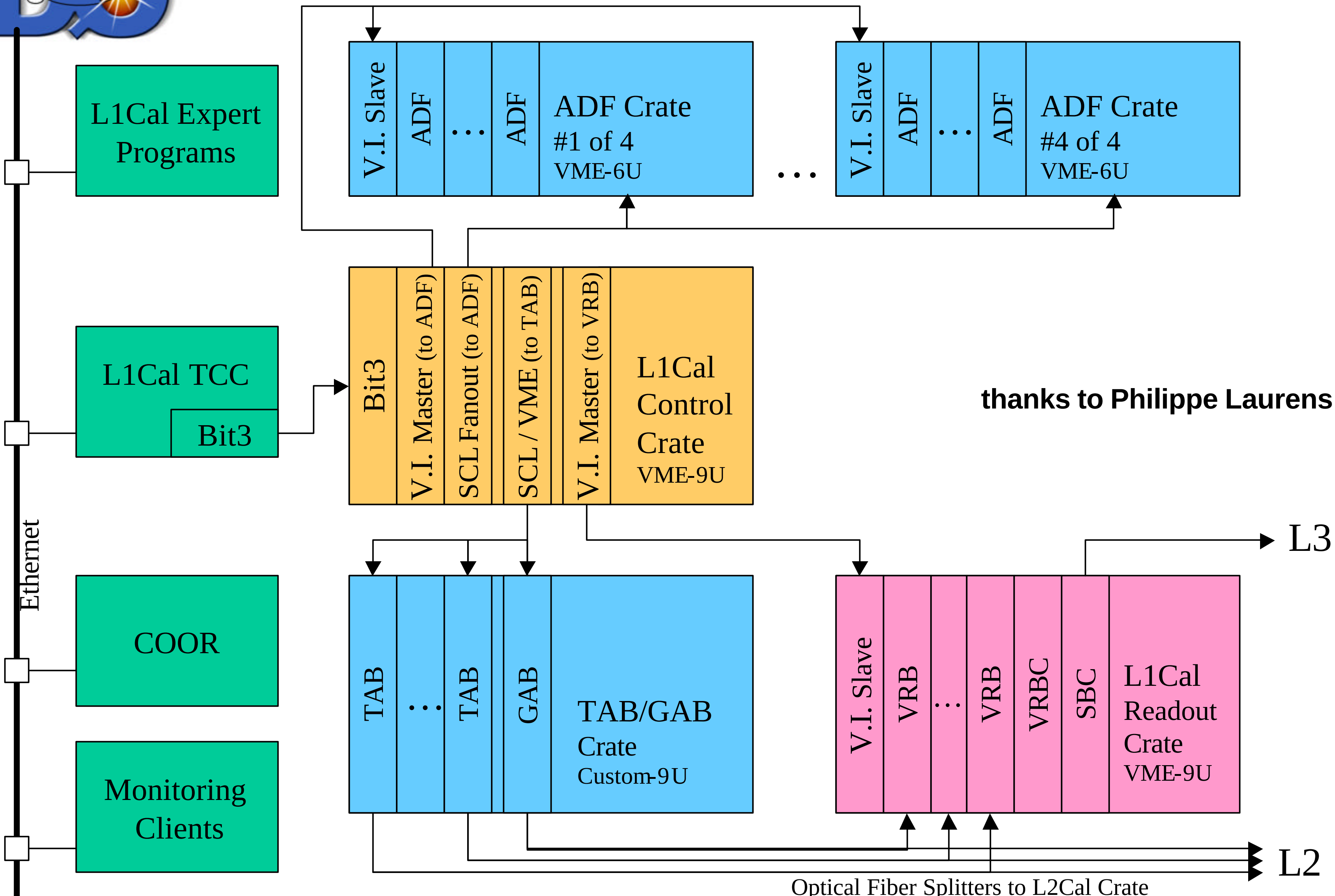
- **Rise time too long for operation at 132 ns:**

  Let E=energy deposited for BC #N: 75% of E observed at BC #N-1: can cause fake trigger at BC #N-1 that causes a veto for BC #N which is lost!

- **Long tail: 80% of max after 132 ns; 20% after 396 ns**

  -> Digital Signal Processing

Run IIb L1 Calorimeter Trigger Control Path



thanks to Philippe Laurens

P. Laurens
Rev: 08-Oct-2003